Diagnosing Single Faults in Fanout-Free Combinational Circuits

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Abstract—**We show how to construct, in a simple manner, a test set having $n + 1$ tests for a fanout-free combinational circuit with n primary inputs which distinguishes (diagnoses) nonequivalent single faults. This result is an improvement over the upper bound in [1, Theorem 3.9] of $n + g$ (g is the number of primary input gates) and the upper bound in [3, Theorem 4], [5] of $2n$ for the least number of tests required to distinguish among nonequivalent single faults.**

Index Terms—**Algorithm, diagnosing single faults, fanout-free combinatorial circuits, stuck line fault, test set.**

I. Introduction

Throughout this paper we shall be talking about the standard stuck line fault model. The reader should consult [1], [2], or [3] if additional information is desired.

We say that a test set T diagnoses single faults if given any two nonequivalent faults (nonequivalent means that they differ on some input) we can find a test $t \in T$ on which the two faults differ. Clearly, we cannot expect to do any better than to determine the equivalence class of the fault. The algorithm we present produces a single fault diagnostic test set of size $n + 1$ where n is the number of inputs of the fanout-free combinational circuit. This is an improvement over the upper bounds of [1], [3], and [5].

Since the structure of single faults is known for fanout-free combinational circuits (see [2, p. 1501]), we will not bother to relate the test set we construct to particular faults. Such a relationship is implicit in the algorithm we give and can be worked out by the interested reader.

II. The Algorithm

Given a test set T for a given circuit, we use $T^u(T^z)$ to denote those tests on which the fault-free circuit has the value 1(0). The algorithm proceeds inductively. We assume that we know what the single fault diagnostic test sets look like on each of the input lines to a gate G, and then we produce a single fault diagnostic test set for the circuit having G as its output gate. Furthermore, to simplify discussion, we will just write out the algorithm in detail for the case where G is a k input AND gate G.

We will use $l_1, \cdots, l_k$ to denote the input lines of G, and $T_1, \cdots, T_k$ to denote single fault diagnostic test sets for the circuits for which $l_1, \cdots, l_k$ (respectively) function as output lines. Furthermore, we let f_i $(i = 1, \cdots, k)$ denote the Boolean function computed by the fault-free circuit for which l_i is the output line and n_i is the number of inputs feeding l_i. Note that each $f_i \not\equiv 0, 1$; thus, $T_i^u \neq \emptyset \neq T_i^z$. Thus, in the absence of faults, the output of G should produce the function $f = f_1 \wedge \cdots \wedge f_k \not\equiv 0, 1$. One additional notational convention is that for $t_i \in T_i$ we use $(t_1, \cdots, t_k)$ to denote the test that consists of simultaneously applying t_i to the inputs feeding l_i for all i.

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With everything as described above, let u_i be an arbitrary member of T_i^u and define

$$T^u = \{(t, u_2, \cdots, u_k) \mid t \in T_1^u\} \cup \cdots \cup \{(u_1, \cdots, u_{k-1}, t) \mid t \in T_k^u\}$$

$$T^z = \{(t, u_2, \cdots, u_k) \mid t \in T_1^z\} \cup \cdots \cup \{(u_1, \cdots, u_{k-1}, t) \mid t \in T_k^z\}$$

and

$$T = T^u \cup T^z.$$

Note that T is very close to the set produced by Procedure 2 in [5].

We now have the following theorem.

Theorem: T is a single fault diagnosing test set for the circuit ending at G. $|T^u| = \sum_{i=1}^{k} |T_i^u| - k + 1$ and $|T^z| = \sum_{i=1}^{k} |T_i^z|$. Thus, $|T| = \sum_{i=1}^{k} |T_i| - k + 1$.

Proof: If a single fault or no fault occurs in the circuit, then the output of G is one of the functions 0, 1,

$$g_{11} \wedge f_2 \wedge \cdots \wedge f_k,$$
$$g_{12} \wedge f_2 \cdots \wedge f_k, \cdots, g_{1m_1} \wedge f_2 \wedge \cdots \wedge f_k,$$
$$f_1 \wedge g_{21} \wedge f_3 \wedge \cdots \wedge f_k, \cdots, f_1 \wedge g_{2m_2} \wedge f_3 \cdots \wedge f_k, \cdots,$$
$$f_1 \wedge f_2 \wedge \cdots \wedge f_{k-1} \wedge g_{km_k}, \quad f_1 \wedge \cdots \wedge f_k$$

where g_{ip} $(p = 1, \cdots, m_i)$ are the nonequivalent nonzero functions which can occur as a result of a single fault in the circuit having l_i as an output line (see [2], [4]).

Since each $f_1 \wedge \cdots \wedge g_{ip} \wedge \cdots \wedge f_k$ is 0 on any element of the form $(u_1, \cdots, u_{r-1}, t, u_{r+1}, \cdots, u_k)$ with $r \neq i$ and $t \in T_r^z$ and 1 on some element of the form $(u_1, \cdots, u_{i-1}, t, u_{i+1}, \cdots, u_k)$ with $t \in T_i$ (since T_i distinguishes g_{ij} from 0), T clearly distinguishes between 0, 1 and the other faults. Since $T^z \neq \emptyset \neq T^u$, T diagnoses the faults 0, 1.

We now show that if θ, γ are two distinct functions in the list given at the start of the proof such that $\theta, \gamma \not\equiv 0, 1$, then some element of T causes them to assume different values. There are two cases to consider.

Case 1: θ and γ differ only in the ith conjunct. Here it is clear that T distinguishes between θ and γ since some $t \in T_i$ distinguishes between the ith conjunct of θ and γ, whence $(u_1, \cdots, u_{i-1}, t, \cdots, u_k)$ distinguishes between θ and γ. In particular, this shows that T detects all single faults (it actually detects all multiple faults; see [2], [4]).

Case 2: θ and γ differ in the ith and jth conjuncts with $i \neq j$. Thus, we may assume that $\theta = f_1 \wedge \cdots \wedge g_{ip} \wedge f_{i+1} \wedge \cdots \wedge f_k$ and $\gamma = f_1 \wedge \cdots \wedge g_{jq} \wedge f_{j+1} \wedge \cdots \wedge f_k$. Note that θ is 0 on

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$$T^z - \{(u_1, \cdots, u_{i-1}, t, u_{i+1}, \cdots, u_k) \mid t \in T_i^z\}$$

and γ is 0 on

$$T^z - \{(u_1, \cdots, u_{j-1}, t, u_{j+1}, \cdots, u_k) \mid t \in T_i^z\}.$$

Since the union of the two sets in the previous sentence is all of T^z, either some element of T^z distinguishes between θ and γ or θ and $\gamma \equiv 0$ on T^z. In the first instance, we are done. In the second, we continue the argument as follows.

First note that if γ and θ are identically 0 on T^z, then $g_{ip} \equiv 0$ on T_i^z and $g_{jq} \equiv 0$ on T_j^z. Since $g_{ip} \not\equiv f_i$, $g_{ip} \equiv 0$ on T_i^z and T_i diagnoses all faults which can occur at l_i, there exist $t_1, t_2 \in T_i^u$ such that $g_{ip}(t_1) = 1$ and $g_{ip}(t_2) = 0$. Let $t_1^* = (u_1, \cdots, u_{i-1}, t_1, u_{i+1}, \cdots, u_k)$ and $t_2^* = (u_1, \cdots, u_{i-1}, t_2, u_{i+1}, \cdots, u_k)$. If $g_{jq}(u_j) = 0$, then $\theta(t_1^*) = 1$ while $\gamma(t_1^*) = 0$. If $g_{jq}(u_j) = 1$, then $\theta(t_2^*) = 0$ while $\gamma(t_2^*) = 1$. Since $t_1^*, t_2^* \in T^u$, T distinguishes between θ and γ.

Finally, note that $|T^z|$ is just the sum of the $|T_i^z|$ since all the subsets we used to create T^z are disjoint, while $|T^u|$ is just the sum of the $|T_i^u|$ minus $(k - 1)$ since the element $(u_1, \cdots, u_k)$ belongs to each of the subsets we used to create T^u. □

Corollary: A fanout-free combinational circuit with n primary inputs has a single fault diagnosing test set containing exactly $n + 1$ tests.

Proof: The proof proceeds by induction on n. For $n = 1$ or 2, the result is obvious. Now consider the case of the AND gate described earlier. By induction we choose T_i so that $|T_i| = n_i + 1$ where n_i is the number of primary inputs feeding the line l_i. By the theorem $|T| = \sum_{i=1}^{k} (n_i + 1) - k + 1 = (\sum_{i=1}^{k} n_i) + 1 = n + 1$. The proof for other kinds of gates is essentially identical. □

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